REMARKS

The above amendments and following remarks are submitted in response to the Official Action of the Examiner mailed September 28, 2004. Having addressed all objections and grounds of rejection, claims 1-25, being all the pending claims, are now deemed in condition for allowance. Entry of this amendment and reconsideration to that end is respectfully requested.

Claims 1, 6-7, 11, 16, and 21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,850,534, issued to Kranich (hereinafter referred to as "Kranich") in view of U.S. Patent No. 5,228,135, issued to Ikumi (hereinafter referred to as "Ikumi"). This ground of rejection is respectfully traversed for the following reasons.

A key requirement of MPEP 2143 is that the alleged combination (i.e., Kranich in view of Kumar in this case) must contain all of the claimed limitations. Each of these claims (and indeed all pending claims) requires a dedicated interface from the system bus to the level two cache tag storage which is separate from the path from the system bus to the level two cache data storage. The importance of this feature is found in Applicants' specification in numerous places including page 7, lines 13-18.

The Examiner admits that Kranich does not have this feature, stating:

> However, Kranich does not specifically teach a system memory bus coupled to said data memory via a first dedicated path, and to said tag memory via a second dedicated path as recited in the claim.

This feature is important in Applicants' system as stated in the specification and has been discussed a number of times in the prosecution of this application.

The efficiencies derived from this feature are only present when the tag memory is multi-ported. That means that the tag memory can overlap responses to activity from its processor and to memory bus SNOOPing. As illustrated in Fig. 4 of Applicants' disclosure, SLC Tag Storage 72 has a first path 92 which interfaces to the Control Logic 62 and a second path 82 which couples directly to memory bus 80.

Kranich does not have this feature, as admitted by the Examiner, and cannot have the feature, because the Level 2 Tag Array 203 is single ported and can only interface with Level 2 Cache Controller 201. It is single ported because, as taught by Kranich at column 3, lines 34-44:

> Each cache level greater than level one contains a hit array for each storage location within the cache. This hit array indicates whether the information at a particular storage location in the current level cache also resides in the cache one level below the current level cache in the chain of caches assigned to the same processor. According to another aspect of the invention, a multi-level cache system for reducing snooping overhead includes a highest level cache connected to a shared memory bus.

In other words, Kranich teaches a hierarchy of single ported higher-level cache memories wherein only the highest level snoops the memory bus. All other levels snoop only the nest highest level. Thus, Kranich does not have the claimed feature and cannot use employ it without changing the entire architecture taught.

Furthermore, the finding of this feature in Ikumi is clearly erroneous. The Examiner states:

> Ikumi discloses a cache memory control unit having a system memory bus interface unit providing first dedicated path between a system bus and a cache storage [*dedicated path directly coupled between cache memory 14 and bus interface 16*; Fig. 3], and a second dedicated path between a system bus and a tag storage [*snoop address path independently and directly coupled to tag memory 15 and bus interface 16*, Fig. 7[1]],....

Unlike the claimed invention, Ikumi shows only one interface to System Bus 17 in Fig. 3. This interface is System Bus Interface 16. Ikumi does not describe System Bus Interface 16 in any detail. Therefore, Ikumi shows at most dedicated paths to System Bus Interface 16. It does not meet the limitations of the claims which require separate and dedicated paths to the "system memory bus".

In addition, the alleged combination of Kranich and Ikumi does not meet the other two requirements of MPEP 2143, which require a showing of "motivation" and "reasonable likelihood of

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[1]It is assumed that the Examiner means Fig. 3, and that Fig. 7 is merely a typographical error, because Ikumi has no Fig. 7.

success". In attempting to show motivation, the Examiner concludes:

> ....an artisan would have been motivated to use a system memory bus coupled to a data memory via a first dedicated path, and to a tag memory via a second dedicated path in the system of Kranich.

As explained above, because Kranich has a single ported Level 2 Tag Array 203, it would derive no benefit from such a modification. Furthermore, to modify Kranich benefit from the feature would preclude the specific teaching of Kranich to utilize identical higher level cache memories wherein only the highest level cache memory snoops the system memory bus.

The Examiner has not addressed the reasonable likelihood of success. However, it is clearly apparent from Fig. 2 of Kranich that there is not even anywhere to couple the dedicated memory bus interface alleged by the Examiner. Thus, he could not show reasonable likelihood of success as mandated by MPEP 2143.

The claims, though deemed to be patentable for these reasons, have been slightly amended above to make these distinctions even more explicit. The rejection of claims 1, 5-7, 11, 16, and 21, and all claims depending therefrom, is respectfully traversed as based upon clearly erroneous findings of fact and for failure to present a *prima facie* case of obviousness as specified by MPEP 2143.

Claims 2 and 8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Ikumi and further in

view of U.S. Patent No. 5,426,765, issued to Stevens et al (hereinafter referred to as "Stevens"). This ground of rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness as specified by MPEP 2143.

To the alleged combination of the incompatible teachings of Kranich and Ikumi which is unmotivated and inoperative as explained above, the Examiner alleges the further combination with Stevens, which is incompatible with both Kranich and Ikumi. Stevens is not even related to the Central Processing Units of Kranich and Ikumi. Instead, Stevens operates at the microprocessor level. Column 1, lines 9-10, states:

> The present invention relates to microprocessor cache subsystems in computer systems....

Because Stevens is concerned with microprocessors instead of central processing systems, it is restricted to component characteristics which do not make sense in the context of Kranich and Ikumi. The Abstract of Stevens begins:

> A method for arbitrating between processor and host bus snoop accesses to a cache subsystem in a multiprocessor system <u>where the processor does not allow for processor cycle aborts</u>. (Emphasis added)

As a result, Stevens teaches that his disclosure is limited to microprocessors having characteristics not found in or applicable to the CPU's of Kranich and Ikumi. For these reasons, one would be neither motivated to make the alleged combination, nor would the alleged combination have a reasonable likelihood of success.

The rejection of claims 2 and 8, and claims depending therefrom, is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness.

Claims 3-5 and 22-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Ikumi in view of Stevens and further in view of U.S. Patent No. 6,353,877, issued to Duncan (hereinafter referred to as "Duncan"). This ground of rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness as required by MPEP 2143.

To the unmotivated and inoperative alleged combination of the incompatible Kranich, Ikumi, and Stevens references, the Examiner alleges the further combination of Duncan. Unlike Kranich, Ikumi, and Stevens, Duncan's architecture is optimized about the use of non-cached, Input/Output devices. The Abstract of Duncan states:

> A method for improving partial cache line writes from I/O devices to the central processing units incorporates cache coherency protocol and an enhanced invalidation scheme to ensure atomicity (sic), which minimizes the bus utilization.

Any fair reading of Duncan indicates that the architectural features of Duncan relied upon by the Examiner to reject claims 3-5 and 22-23, exist to accommodate the "non-cached I/O devices" which are unique to Duncan and not found in Kranich, nor Ikumi, nor Stevens. Therefore, there is certainly no motivation to make

the alleged combination and it presents no likelihood of success, a legal requirement not addressed by the Examiner.

Therefore, the rejection of claims 3-5 and 22-23 is respectfully traversed for failure to present a *prima facie* case of obviousness.

Claim 9 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Ikumi in view of Stevens and further in view of U.S. Patent No. 6,457,087, Fu (hereinafter referred to as "Fu"). This ground of rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness.

Having not met the requirements of MPEP 2143 in showing motivation, reasonable likelihood of success, or all claim limitations for the alleged combination of Kranich, Ikumi, and Stevens as to claim 8, from which claim 9 depends, the Examiner alleges the further combination with Fu. In addition to the compounded issues with regard to motivation and reasonable likelihood of success, the alleged combination does not have the unique claim limitations of claim 9 which requires:

> a. A level one tag memory located within said level one cache memory; and
> b. A duplicate tag memory within said level two cache memory which maintains <u>a duplicate of information within said level one tag memory</u>. (Emphasis added)

In making his citation of this rather strange alternative embodiment of Duncan, the Examiner states:

[L2 duplicate tag memory 232 contains duplicate tags for each data block in L2 which contains data that is stored in L1; Fig. 5C] (emphasis added)

Thus, the claim requires duplicate L1 tags and Duncan has duplicate L2 tags. The rejection of claim 9 is respectfully traversed.

Claim 10 has been rejected under 35 U.S.C. 103(a0 as being unpatentable over Kranich in view of Ikumi in view of Stevens in view of Fu and further in view of Duncan. This ground of rejection is respectfully traversed for failure to present a *prima facie* case of obviousness.

To the completely untenable alleged combination of Kranich and Ikumi and Stevens and Fu, the Examiner alleges the further combination with Duncan. As explained above, the architectural features relied upon by the Examiner exist to service "non-cached Input/Output devices" which are not found in nor contemplated by Kranich, Ikumi, Stevens, or Fu. The rejection of claim 10 is respectfully traversed as rejected on an alleged combination which is unmotivated, having no reasonable likelihood of success, and not containing all of the claimed elements.

Claims 12 and 17 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Ikumi, and further in view of Stevens. The rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness.

As with the rejection of claims 2 and 8, the Examiner has failed to show that the alleged combination is motivated, has a reasonable likelihood of success, and meets all of the claimed elements. The rejection of claims 12 and 17 is respectfully traversed.

Claim 13 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Ikumi in view of Stevens and further in view of Fu. This ground of rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness. As explained above with respect to the rejection of claim 9, Fu discloses duplicate storage of L2 tags, rather than the claimed duplicate storage of L1 tags. The rejection of claim 13 is respectfully traversed.

Claims 14 and 15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Ikumi in view of Stevens in view of Fu and further in view of Duncan. The rejection of claims 14 and 15 is respectfully traversed for failure to meet any of the three requirements of a *prima facie* case of obviousness as required by MPEP 2143 for the reasons provided above.

Claim 18 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Stevens and further in view of Ikumi. This ground of rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of

obviousness. The claim requires "directly coupling to said bussing means". As explained above, Ikumi teaches separate coupling to the bus interface, not to the bus. The rejection of claim 18 is respectfully traversed.

Claim 19 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Stevens in view of Ikumi and further in view of Fu. Claim 19 depends from claim 18 and further requires a "recording means" and a "duplicating means". For both elements, it is the L1 tags which are recorded and the L1 tags which are duplicated. As the Examiner is fully aware, the alleged combination does not contain these limitations. Furthermore, the Examiner acknowledges this deficiency but none the less cites Fu to show duplicate L2 tags. As a result, the rejection of claim 19 is respectfully traversed for failure of the Examiner to make any of the three showings required by MPEP 2143.

Claim 20 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Stevens in view of Ikumi in view of Fu and further in view of Duncan. This rejection is respectfully traversed for failure to meet any of the three showings of MPEP 2143 to present a *prima facie* case of obviousness for the reasons discussed at length above.

Claims 24-25 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich in view of Ikumi in view of

Stevens in view of Duncan and further in view of U.S. Patent No. 5,692,152, issued to Cohen et al (hereinafter referred to as "Cohen"). Cohen is concerned with pipelined microprocessors having little to do with the central processing units utilized in the other references. As a result, the alleged combination is neither motivated nor reasonably likely to succeed. The rejection of claims 24-25 is respectfully traversed.

Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-25, being the only pending claims.

Please charge any deficiencies or credit any overpayment to Deposit Account No. 14-0620.

Respectfully submitted,

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By their attorney,

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